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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,796	01/11/2002	David Glen White	RCA89647	5621

7590 12/01/2005

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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,796	WHITE ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/11/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-5 in the reply filed on October 31, 2005 is acknowledged. The traversal is on the ground(s) that claims 1-11 do not form three groups of inventions but rather form a single general inventive concept under PCT Rule 13.1 because independent claim 1 embodies the present concept and special technical feature thereof by having the limitation of allowing coupling of a noise intolerant device with a processor of an electrical device only when the processor is communicating with the noise intolerant device, independent claim 6 also embodies the present concept and special technical feature thereof by claiming a television receiver having the limitation of allowing coupling of a phase-lock loop (embodiment of a noise intolerant device) to a processor only when the processor is communication with the phase-lock loop, and independent claim 8 also embodies the present concept and special technical feature thereof as a method in a tuner of a television that includes of the limitation of allowing coupling of a phase-lock loop of the television tuner (embodiment of a noise intolerant device) to a processor thereof only when the processor is communicating with the phase-lock loop.

This is not found persuasive because it is noted that claims 6-11 can be group in one group because they have a single general inventive concept "allowing coupling of a phase-lock loop to a processor only when the processor is communication with the phase-lock loop" and claims 1-5 can be group in other group because they embodies different general invention concept "allowing coupling of a noise intolerant device with a

processor of the electrical circuit/device only when the processor is communicating with the noise intolerant device". It is further noted that the claimed "noise intolerant device" and the claimed "the phase-lock loop" are two different inventive concepts because the "noise intolerant device" may not contain "the phase-lock loop" and the "phase-lock loop" may not be used in the "noise intolerant device".

2. Claims 6-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on October 31, 2005.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

3. Claim 3 is objected to because of the following informalities: In lines 3, 6 and 7, the phrase "said IIC bus expander" should changed to "a IIC bus expander". Appropriate correction is required.

For rejection purposes, the examiner assumes that the dependent claim 3 is depend to claim 2.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipate by Ishida Akira (JP Publication No. 60144857 A).

In considering claim 1, Ishida Akira discloses all the claimed subject matter, note 1) the claimed a processor for producing clock and data signals and a control signal is met by the CPU 2 (Fig. 2, page 3, lines 15-29), 2) the claimed a digital bus that couples said clock and data signals to a buffer is met by the data bus 5 or 6 (Fig. 2, page 3, lines 15-29), 3) the claimed where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device is met by the bus buffer 1 which separates or connects the data bus 6 (connected to peripheral element 8) from or to data bus 5 (Fig. 2, page 3, lines 15-29).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida Akira (JP Publication No. 60144857 A) in view of Tults et al (US Patent No. 6,693,678 B1).

In considering claim 2, Ishida Akira discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein said digital bus is an inter integrated circuit bus, and the apparatus further comprises an IIC bus expander for transferring said control signal to said buffer. Tults et al teach that in a conventional data bus system such as the IIC bus system shown in Fig. 1, master device 2 is connected to slave device 4 (designed slave #1 by IIC bus 6 (Figs. 1 and 3, col. 3, lines 40-62). Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the IIC bus as taught by Tults et al into Ishida Akira's system in order to transfer the data and clock signals which large loads at high speed to perform the communication between master and slave devices as fast as possible.

Additionally, the capability of using an IIC bus expander is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the old and well known of using an IIC bus expander into Ishida Akira's system in order to expand the bandwidth of the IIC bus.

In considering claim 3, Tults discloses all the claimed subject matter, note 1) the claimed wherein the digital bus comprises an IIC bus having a clock signal path for transferring clock pulses from said processor to said clock inputs of said IIC bus expander and said buffer is met by the bus line SCL (Fig. 3, col. 4, lines 41-58), 2) the claimed a data signal path for transferring data from said processor on said data signal path during each of said clock pulses on said clock signal path to said clock and data

inputs of said IIC bus expander and said buffer is met by the bus line SDA (Fig. 3, col. 4, lines 41-58), and 3) the claimed wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device from said IIC bus and said processor is met by the tri-state buffers 15 and 16 (Fig. 3, col. 4, line 59 to col. 6, line 4).

In considering claim 4, the claimed wherein said noise intolerant device comprises: a tuner, coupled to said clock and data outputs of said buffer device, having a phase-lock loop for generating frequency variable tones, and a down-converter coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal is met by the tuner of the television receiver (col. 1, line 11 to col. 2, line 28 of Tult et al).

Allowable Subject Matter

8. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Belotserkovsky (US Patent No. 6,678,012 B1) discloses LNB drift search system for DBS products.

Ben-Efraim et al. (US Patent No. 5,870,439) disclose satellite receiver tuner chip having deduced digital noise interference.

Ishida et al. (US Patent No. 5,142,671) disclose plural cache architecture for real time multitasking.

Moelands et al. (US Patent No. 4,689,740) disclose two-wire bus-system comprising a clock wire and a data wire for interconnecting a number of stations.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT
November 25, 2005

Trang U. Tran
Examiner
Art Unit 2614